REMARKS

In sections 1-5 of the Office Action, the Examiner rejected claims 15, 26, and 38 under 35 U.S.C. §102(b) as being anticipated by the Williams patent.

The Williams patent discloses an adaptive equalizer 100 that includes an analog-to-digital converter 101, a finite impulse response (FIR) filter 106, and a digital-to-analog converter 105. The FIR filter 106 corrects for various signal impairments such as multipath (ghosts) and includes time delay elements 102, programmable multipliers 103, and a summing circuit 104. The FIR filter 106 performs a convolution based on tap coefficients C(k) applied by the multipliers 103 to input samples x(n) so as to produce output samples y(n), where k is the tap number, N+1 is the number of taps, n is the time sample index. The equalizer 100 has real-only tap coefficients.

The Williams patent also discloses an adaptive equalizer 200 with complex taps. The adaptive equalizer structure 200 has a real-to-real section 202, an imaginary-to-real section 203, a real-to-imaginary section 204, and an imaginary-to-imaginary section 205. The adaptive equalizer 200 also includes a first analog-

to-digital converter 201 that receives the real portion of an input signal and that is coupled to the real-to-real FIR filter 202 and to the real-to-imaginary FIR filter 204. A second analog-to-digital converter 211 receives the imaginary portion of the input signal and is coupled to the imaginary-to-real FIR filter 203 and to the imaginary-to-imaginary FIR filter 205. The outputs of the FIR filters 202 and 203 are coupled to a subtractor 206, and the output of subtractor 206 is coupled to digital-to-analog converter 208. The output of digital-to-analog converter 208 provides a ghost canceled in-phase signal. The outputs of the FIR filters 204 and 205 are coupled to a summer 207, and the summer 207 provides the summed output to a digital-to-analog converter 209 which provides a ghost canceled quadrature signal.

Independent claim 15 is directed to a method of substantially eliminating a ghost of a received main signal and reducing noise enhancement. The received main signal and the ghost are processed along n paths to produce n processed main signals and n processed ghosts, where n > 3. Each of the n paths includes a corresponding finite filter. The processing along each of the n paths does not substantially eliminate the

ghost, and the processing along at least some of the n paths includes shifting data. The n processed main signals and the n processed ghosts are added such that, because of the addition of the n processed main signals and the n processed ghosts, the ghost of the received main signal is substantially eliminated.

The Examiner relies on Figure 1 in the rejection of independent claim 15. However, independent claim 15 requires that each of the n paths includes a corresponding finite filter. Figure 1 shows only a single filter 106.

Moreover, independent claim 15 requires the adding of the n processed main signals and the n processed ghosts where n > 3. Figure 2 of the Williams patent does not show the adding of n signals where n > 3.

For these reasons, the Williams patent does not anticipate independent claim 15.

Independent claim 26 is directed to an equalizer that comprises n processing paths arranged to process the blocks of data, n - 1 data shifters, n finite filters, and an adder. The n processing paths are arranged to process blocks of data. Each of the n - 1 data shifters is in a corresponding one of the n processing paths so that one of the n processing paths

has no data shifter. Each of the n finite filters is in a corresponding one of the n processing paths, and each of the n finite filters applies a corresponding set of finite filter coefficients to the blocks of data. Ghosts of the blocks of data are not eliminated as a result of the application of the sets of finite filter coefficients corresponding to the n finite filters, and n > 2. The adder adds outputs from the n processing paths, and the addition eliminates ghosts of the blocks of data.

The Examiner relies on Figure 1 in the rejection of independent claim 26. However, independent claim 26 requires that each of the n paths includes a corresponding finite filter. Figure 1 shows only a single filter 106.

Moreover, independent claim 26 requires that each of the n paths except one has a data shifter. Figure 2 of the Williams patent does not show this arrangement.

Furthermore, independent claim 26 requires and adder that adds outputs from the n processing paths, where n > 2. The subtractor 206 shown in Figure 2 of the Williams patent processes signals in only two paths, and the adder 207 shown in Figure 2 of the Williams patent likewise processes signals in only two paths.

For these reasons, the Williams patent does not anticipate independent claim 26.

Because the Williams patent does not anticipate independent claim 26, the Williams patent likewise does not anticipate dependent claim 38.

In sections 6-10 of the Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. §103(a) as being unpatentable over the Williams patent in view of the Zheng patent.

Independent claim 1 is directed to a method of equalizing a signal. Data in a series of input data blocks is shifted to the left, and each of the left shifted data blocks is multiplied by a first set of equalizer coefficients to provide first adjusted output data blocks. This first multiplication does not result in a full solution to ghosts. Each of the un-shifted input data blocks is multiplied by a second set of equalizer coefficients to provide second adjusted output data blocks. This second multiplication does not result in a full solution to ghosts. The data in each of the input data blocks of data is shifted to the right, and each of the right shifted input data blocks is multiplied by a third set of equalizer coefficients to provide third adjusted output data blocks. This third multiplication

does not result in a full solution to ghosts. Corresponding ones of the first, second, and third adjusted output data blocks are added so as to provide a substantially full solution to ghosts.

The Williams patent does not disclose shifting input data blocks to the left and to the right.

Moreover, the Williams patent does not disclose multiplying left shifted input data blocks by a first set of equalizer coefficients to provide first adjusted output data blocks while multiplying un-shifted input data blocks by a second set of equalizer coefficients to provide second adjusted output data blocks while multiplying right shifted input data blocks by a third set of equalizer coefficients to provide third adjusted output data blocks.

Furthermore, the Williams patent further does not disclose adding corresponding ones of the first, second, and third adjusted output data blocks.

The Examiner relies on the Zheng patent to show signal shifting. The shifting disclosed in the Zheng patent is for synchronization purposes. That is, the shifting disclosed in the Zheng patent is used to synchronize the receiver symbol rate with the transmitter symbol rate. Therefore, all taps are shifted to the

right or left and are then applied to data. The Zheng patent does not disclose shifting some of the taps to the left and applying the left shifted taps to the input data while shifting others of the taps to the right and applying the right shifted taps to the input data while not shifting still others of the taps and applying the un-shifted taps to the input data.

More specifically, the Zheng patent discloses a modem receiver 100 that recovers output data d(n) from a complex baseband signal. The complex baseband signal is sampled by a sampler 102 to produce input data x(n). The input data x(n) is fed into an adaptive equalizer 104 with fractionally spaced taps W(z). The adaptive equalizer 104 is a transversal finite-impulse-response (FIR) filter. The taps of the adaptive equalizer 104 are used to filter the input data x(n) in time coordination with a fixed sample clock rate to generate the equalized data y(n). The equalized data y(n) at the output of the adaptive equalizer 104 are down-sampled by a down-sampler 106 to generate candidate output data y'(n) which is supplied to a decision logic/decoder 108 to produce the output data d(n). The taps of the adaptive equalizer 104 are adjusted in response to an error signal generated by a subtractor 110 that forms the difference between d(n)

and y'(n). A timing indicator 112 correlates d(n) and x(n) at three indices around the initial peak position k which is established during an initial training of a modem connection. The timing indicator circuit 112 outputs a signal to activate a timing recovery control 114 when the amplitude peak of the calculated correlations has shifted away from the initial position k. The timing recovery control 114 initiates timing recovery to advance or retard the equalized data y'(n) by shifting the taps of adaptive equalizer 104 to the left or right and by advancing or retarding the equalizer output in response to the timing indicator output signal. As a result, the receiver symbol rate is increased or decreased to correspond to the transmitter symbol rate without introducing any jitter in the equalized data y(n).

Thus, the Zheng patent discloses shifting all of the taps to the left, or shifting all of the taps to the right, or not shifting any of the taps. The Zheng patent does not disclose or suggest shifting some of the taps to the left, shifting others of the taps to the right, and not shifting still others of the taps at all, and then multiplying data by the left shifted taps, by the right shifted taps, and by the un-shifted taps.

Accordingly, unlike the requirements of independent claim 1, the Zheng patent does not disclose or suggest shifting all of the taps to the left, suggest multiplying left shifted data blocks by a first set of equalizer coefficients, multiplying un-shifted input data blocks by a second set of equalizer coefficients, and multiplying right shifted input data blocks by a third set of equalizer coefficients.

For this reason, the Williams patent and the Zheng patent cannot be combined to meet the limitations of independent claim 1.

Accordingly, independent claim 1 is not unpatentable over the Williams patent in view of the Zheng patent.

Because independent claim 1 is not unpatentable over the Williams patent in view of the Zheng patent, dependent claim 2 likewise is not unpatentable over the Williams patent in view of the Zheng patent.

In sections 11-13 of the Office Action, the Examiner rejected claims 3, 4, 9, and 14 under 35 U.S.C. §103(a) as being unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

As discussed above, neither the Williams patent nor the Zheng patent discloses or suggests multiplying left shifted data blocks by a first set of equalizer coefficients, multiplying un-shifted input data blocks by a second set of equalizer coefficients, and multiplying right shifted input data blocks by a third set of equalizer coefficients.

Likewise, the Yamasaki patent does not disclose or suggest multiplying left shifted data blocks by a first set of equalizer coefficients, multiplying un-shifted input data blocks by a second set of equalizer coefficients, and multiplying right shifted input data blocks by a third set of equalizer coefficients.

Instead, the Yamasaki patent discloses a system including an AGC amplifier 401, an equalizer 403, and a Viterbi-like decoder 406. The Viterbi-like decoder 406 has a maximum-likelihood estimator 407, a decoder 409, and a state feedback block 412. The AGC amplifier 401 sets the input signal amplitude so that an input signal 400 is sampled at preset levels. The equalizer 403 equalizes the signal to the desired partial response waveform. The maximum-likelihood estimator 407 processes the sample values through a set of decision functions to generate a set of metrics. These metrics are provided to

the decoder 409 which compares the metrics with state dependent detection threshold values. The decoder 409 determines the detected data value and provides the detected data as an output signal 410. Concurrently, the decoder 409 provides an update signal 411 to the state feedback block 412 to update the detection state of the decoder 409. The state feedback block 412 provides the new state as a signal 413 to the decoder 409 for use in determining the detection thresholds for the next set of detection values.

Consequently, because neither the Williams patent, nor the Zheng patent, not the Yamasaki patent discloses or suggests multiplying left shifted data blocks by a first set of equalizer coefficients, multiplying un-shifted input data blocks by a second set of equalizer coefficients, and multiplying right shifted input data blocks by a third set of equalizer coefficients, independent claim 1 is not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

Because independent claim 1 is not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent, dependent claims 3, 4, 9, and 14 likewise are not unpatentable over the

Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

In section 14 of the Office Action, the Examiner rejected claims 16 and 35 under 35 U.S.C. §103(a) as being unpatentable over the Williams patent in view of the Zheng patent.

As discussed above, independent claim 15 requires that each of the n paths includes a corresponding finite filter, and Figure 1 of the Williams patent shows only a single filter 106. As also discussed above, independent claim 15 requires the adding of the n processed main signals and the n processed ghosts where $n > 3$, and Figure 2 of the Williams patent does not show the adding of n signals where $n > 3$.

Similarly, the Zheng patent does not disclose n paths each including a corresponding finite filter.

Consequently, because neither the Williams patent nor the Zheng patent discloses or suggests the invention of independent claim 15, the combination of the Williams patent and the Zheng patent cannot disclose or suggest the invention of independent claim 15. Therefore, independent claim 15 is not unpatentable over the Williams patent in view of the Zheng patent.

Because independent claim 15 is not unpatentable over the Williams patent in view of the Zheng patent, dependent claim 16 likewise is not unpatentable over the Williams patent in view of the Zheng patent.

Moreover, as discussed above, independent claim 26 recites n paths each including a corresponding finite filter with each path except one having a data shifter. As also discussed above, the Williams patent does not disclose n paths each including a corresponding finite filter and does not disclose n paths with each path except one having a data shifter. Similarly, the Zheng patent does not disclose n paths each including a corresponding finite filter and does not disclose n paths with each path except one having a data shifter.

Consequently, because neither the Williams patent nor the Zheng patent discloses or suggests the invention of independent claim 26, the combination of the Williams patent and the Zheng patent cannot disclose or suggest the invention of independent claim 26. Therefore, independent claim 26 is not unpatentable over the Williams patent in view of the Zheng patent.

Because independent claim 26 is not unpatentable over the Williams patent in view of the

Zheng patent, dependent claim 35 likewise is not unpatentable over the Williams patent in view of the Zheng patent.

In sections 15-17 of the Office Action, the Examiner rejected claims 17, 18, 24, 25, 27, 28, and 34 under 35 U.S.C. §103(a) as being unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

As discussed above, independent claim 15 requires that each of the n paths includes a corresponding finite filter, and Figure 1 of the Williams patent shows a single filter 106 only. As also discussed above, independent claim 15 requires the adding of the n processed main signals and the n processed ghosts where n > 3, and Figure 2 of the Williams patent does not show the adding of n signals where n > 3. As further discussed above, the Zheng patent does not disclose n paths with each path including a corresponding finite filter.

Similarly, the Yamasaki patent does not disclose n paths with each path including a corresponding finite filter.

Consequently, because neither the Williams patent nor the Zheng patent nor the Yamasaki patent

discloses or suggests the invention of independent claim 15, the combination of the Williams patent, the Zheng patent, and the Yamasaki patent cannot disclose or suggest the invention of independent claim 15. Therefore, independent claim 15 is not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

Because independent claim 15 is not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent, dependent claims 17, 18, 24, and 25 likewise are not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

Moreover, as discussed above, independent claim 26 recites n paths with each path including a corresponding finite filter and with each path except one having a data shifter. As also discussed above, neither the Williams patent nor the Zheng patent discloses or suggests n paths with each path including a corresponding finite filter and with each path except one having a data shifter. Similarly, the Yamasaki patent does not disclose n paths with each path including a corresponding finite filter and does not disclose n paths with each path except one having a data shifter.

Consequently, because neither the Williams patent nor the Zheng patent nor the Yamasaki patent discloses or suggests the invention of independent claim 26, the combination of the Williams patent, the Zheng patent, and the Yamasaki patent cannot disclose or suggest the invention of independent claim 26. Therefore, independent claim 26 is not unpatentable over the Williams patent in view of the Zheng patent.

Because independent claim 26 is not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent, dependent claims 27, 28, and 34 likewise are not unpatentable over the Williams patent in view of the Zheng patent and further in view of the Yamasaki patent.

In section 18 of the Office Action, the Examiner rejected claims 36 and 37 under 35 U.S.C. §103(a) as being unpatentable over the Williams patent in view of the Zheng patent.

As discussed above, independent claim 26 recites n paths with each path including a corresponding finite filter and with each path except one having a data shifter. As also discussed above, the Williams patent does not disclose or suggest n paths with each path including a corresponding finite filter and with each

path except one having a data shifter. Similarly, the Zheng patent does not disclose n paths with each path including a corresponding finite filter and does not disclose n paths with each path except one having a data shifter.

Consequently, because neither the Williams patent nor the Zheng patent discloses or suggests the invention of independent claim 26, the combination of the Williams patent and the Zheng patent cannot disclose or suggest the invention of independent claim 26. Therefore, independent claim 26 is not unpatentable over the Williams patent in view of the Zheng patent.

Because independent claim 26 is not unpatentable over the Williams patent in view of the Zheng patent, dependent claims 36 and 37 likewise are not unpatentable over the Williams patent in view of the Zheng patent.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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October 29, 2003